

### **Remarks**

Claim 1 was objected to by the Examiner for the inclusion of a repeated phrase in line 10. Claim 1 has been amended to delete that duplication.

**Claims 1-3 and 8-10 were rejected by the Examiner under 35 USC §102(e) as being anticipated by Chong (6,391,731).**

Since Chong ('731) is the primary reference upon which each of the Examiner's specific rejections are based, Chong will be discussed first with respect to the independent claims 1 and 11.

Claim 1 as amended calls for forming a doped polycrystalline silicon gate in a MOS device on a crystalline silicon substrate by:

- a) forming an insulation layer on the silicon substrate;
- b) **forming an amorphous silicon layer on top of and in contact with said insulation layer;**
- c) introducing a dopant in a top surface of said amorphous silicon layer; and
- d) irradiating said top surface of said amorphous silicon layer with a radiation beam to heat said top surface to a temperature between 1150°C and the melting temperature of said silicon substrate to **initiate explosive recrystallization of said amorphous silicon layer from said top surface to the contact with said insulation layer** to transform said amorphous silicon layer into a polycrystalline silicon gate with said dopant distributed uniformly throughout said polycrystalline gate.

Similarly, claim 11 calls for forming a doped polycrystalline silicon gate in a MOS device formed on a top surface of a crystalline silicon substrate by:

- a) forming an insulation layer on silicon substrate;
- b) **forming an amorphous silicon layer on top of and in contact with said insulation layer;**
- c) forming a dopant layer on top of and in contact with said amorphous silicon layer; and
- d) irradiating said amorphous silicon layer with a radiation beam to heat said top surface to a temperature between 1150°C and the melting temperature of said silicon substrate and melt said dopant layer and a top surface layer of said amorphous silicon layer to cause diffusion of said dopant into said top surface layer of said amorphous silicon layer and **explosive recrystallization of said amorphous silicon layer from said top surface to the contact with said insulation layer** to transform said amorphous layer into a polycrystalline silicon gate with said dopant distributed uniformly throughout said polycrystalline gate.

Whereas, Chong states that his process begins with a polysilicon layer 22 overlaying the gate oxide layer 18 (column 2, lines 3-6 and column 2, lines 66 - 67) **unlike claims 1 and 11** that each calls the claimed process starting with **an amorphous silicon layer on an oxide layer**. The gate in the Chong patent is then implanted to form an amorphous layer ONLY in the top portion of the gate (see 34 in Figure 4, and column 3 lines 47-49). Obviously such step is NOT required in claims 1 and 11 since the gate is initially deposited as amorphous silicon THROUGHOUT the entire layer that forms the gate, not only a top layer as in Chong.

Additionally, Chong discloses the heat from the laser radiation pulse enables the **top amorphous layer** of the gate to re-crystallize from the underlying polysilicon layer 22 and become polycrystalline upon **re-crystallization** (column 5, lines 22-25). Applicants' claims 1 and 11 require that the radiation beam to initialize **explosive re-crystallization** of the amorphous silicon **layer from the top surface to the contact**

**with the insulating layer** thereby transforming the entire layer into a polysilicon gate and distributing the dopant uniformly throughout the entire layer.

There is no mention in Chong of “explosive-recrystallization” nor the distribution of a dopant uniformly throughout layers 22 and 34 of his gate structure.

Another difference between Chong and the invention as in Applicants’ claims 1 and 11 is a profound one. Prior to the Applicants’ experiments, one of ordinary skill in the art would have expected that the melt transformation of the entire thickness of an amorphous gate structure would result in the silicon gate curling up into a tube or a number of balls since molten silicon does not “wet” silicon dioxide. To avoid that result, Chong only amorphized the top of his gate while maintaining a lower polysilicon layer of his gate in contact with the silicon dioxide layer. Thus in Chong’s method, the lower remaining polysilicon layer serves as the seed layer when the amorphous layer on top is changed back into polysilicon with a laser pulse.

The methods of Applicants’ claims 1 and 11 when observed in their experiments were not obvious and were quite a surprise to the Applicants’ who are experts in this field. There is no showing or suggestion presented by Chong that anticipates that a complete layer of amorphous silicon resting on silicon dioxide can be transformed into a highly doped polysilicon layer. This result is completely counterintuitive. Clearly Chong teaches avoiding the methods of Applicants’ claims 1 and 11 by his use of a bifurcated gate. Also the result achieved in the Chong patent is not nearly as desirable because it leaves a thin layer of polysilicon next to the gate oxide that is undoped and therefore a poor electrical conductor. In the short time scale of a laser pulse, thermal diffusion will not transport any of the implanted dopant into the polycrystalline material at the bottom of Chong’s gate. This so-called gate depletion region can have a detrimental effect on the threshold voltage and thus seriously compromise the performance of an MOS transistor made using Chong’s method.

For these reasons, amended independent claims 1 and 11 are distinctive, and non-obvious, from the method of Chong.

Thus claims 1-3 and 8-10 are distinguishable from Chong ('731) since claims 2-3 and 8-10 are each dependent from claim 1.

**Claims 11, 15 and 20-22 were rejected by the Examiner under 35 USC §103(a) as being obvious over Chong ('731) in view of Ishida (5,966,605).**

As discussed above, claim 11 is distinguishable from Chong, as are claims 15 and 20-22 since they each are dependent from claim 11.

Thus for this rejection to stand, Ishida must show or suggest all of the features which has been shown above as not being shown or suggested by Chong.

Ishida, like Chong, begins with "...a polysilicon gate 56 which is formed by a CVD process..." (col. 3, line 28). Then at col. 3, lines 36-41 Ishida says:

"After formation of the polysilicon gate 56, the substrate 50 is subjected to a dopant ... to dope the polysilicon gate 56 as represented in Fig. 2b."

No where does Ishida suggest beginning with an amorphous silicon layer on top of and in contact with an insulation layer, or the dispersal of a dopant throughout the entire amorphous silicon layer using explosive recrystallization. Thus since Ishida fails to show or suggest the features in amended claim 11 that are also not shown or suggested by Chong, claim 11 and the claims dependent therefrom, are not obvious from the combination of Chong and Ishida. Therefore claims 11, 15 and 20-22 are patentably distinct from each of Chong and Ishida, whether taken alone or together.

**Claims 12-14 were rejected by the Examiner under 35 USC §103(a) as**

**being obvious over Chong ('731) in view of Ishida in view of Microchip Fabrication – A practical guide to Semiconductor Processing (2000) by Van Zant.**

Since claims 12-14 are each dependent from independent claim 11, they are also patentably distinguishable from the combination of Chong and Ishida as discussed above. Thus for this rejection to stand, Van Zant must show or suggest those features that have been shown as missing from Chong and Ishida, whether taken alone or together.

From a reading of Van Zant, it also does not suggest beginning with an amorphous silicon layer on top of and in contact with an insulation layer, or the dispersal of a dopant throughout the entire amorphous silicon layer using explosive recrystallization as called for in claim 11 from which claims 12-14 depend. Thus since Chong, Ishida and Van Zant each fails to show or suggest the features in amended claim 11 that have been pointed out above, the claims dependent from claim 11 are also not obvious from the combination of Chong, Ishida and Van Zant. Therefore claims 12-14 are patentably distinct from each of Chong, Ishida and Van Zant, whether taken alone or together.

**Claims 16 and 17 where rejected by the Examiner under 35 USC §103(a) as being obvious over Chong ('731) in view of Ishida in view of Talwar ('488).**

Since claims 16 and 17 are each dependent from independent claim 11, they are also patentably distinguishable from the combination of Chong and Ishida. Thus for this rejection to stand, Talwar must show or suggest those features that have been shown above as missing from Chong and Ishida, whether taken alone or together.

The only reason that the Examiner gives for citing Talwar is to show that the laser specifications of claims 16 and 17 had been used previously. Had the Examiner found any of the features that have been shown to be missing from Chong and Ishida, as discussed above, surely Talwar would have been cited for that purpose. Talwar does not disclose or suggest the features that it has been shown above as not being shown by either Chong or Ishida, or their combination. Therefore, claims 16 and 17 are also patentably distinguishable from Chong, Ishida and Talwar whether taken alone or together.

**Claims 18 and 19 were rejected by the Examiner under 35 USC §103(a) as being obvious over Chong in view of Ishida in view of Xiang ('782) in view of Microchip Fabrication – A practical guide to Semiconductor Processing (2000) by Van Zant.**

Since claims 18 and 19 are each dependent from independent claim 11, they are also patentably distinguishable from the combination of Chong, Ishida and Van Zant as discussed above. Thus for this rejection to stand, Xiang must show or suggest those features that have been shown above to be missing from Chong, Ishida and Van Zant, whether taken alone or together.

The only reason that the Examiner gives for citing Xiang is to show the deposition of a metal contact on top of a polycrystalline gate. Had the Examiner found any of the features that have been shown to be missing from Chong, Ishida and Van Zant, as discussed above, surely Xiang would have been cited for that purpose. Xiang does not disclose or suggest the features that it has been shown above are not shown or suggested by any of Chong, Ishida or Van Zant, or their combination. Therefore, claims 18 and 19 are also patentably distinguishable from Chong, Ishida, Xiang and Van Zant taken alone or in any combination.

**Claims 6 and 7 were rejected under 35 USC §103(a) as being obvious over Chong ('731) in view of Xiang (6,159,782) in view of Micron chip Fabrication – A practical guide to Semiconductor Processing (2000) by Van Zant.**

Since claims 6 and 7 are each dependent from independent claim 1, they are also patentably distinguishable from the combination of Chong and Van Zant as discussed above. Thus for this rejection to stand, Xiang must show or suggest those features that have been shown above as missing from Chong and Van Zant, whether taken alone or together.

The only reason that the Examiner gives for citing Xiang is to show the deposition of a metal contact on top of a polycrystalline gate. Had the Examiner found any of the features that have been shown to be missing from Chong and Van Zant, as discussed above, surely Xiang would have been cited for that purpose. Xiang does not disclose or suggest the features that it has been shown above are not shown by either of Chong and Van Zant, or their combination. Therefore, claims 6 and 7 are also patentably distinguishable from Chong, Xiang and Van Zant, alone or in any combination.

**Claim 23 was rejected by the Examiner under 35 USC § 103(a) as being obvious from Chong ('731) in view of Ishida and further in view of Zhang.**

Since claim 23 is dependent from independent claim 11, it is also patentably distinguishable from the combination of Chong and Ishida as discussed above. Thus for this rejection to stand, Zhang must show or suggest those features that have been shown above as being missing from Chong and Ishida, whether taken alone or together.

The only reason that the Examiner gives for citing Zhang is to show the dopant concentrations given in dependent claim 23. Had the Examiner found any of the features that have been shown to be missing from Chong and Ishida, as discussed above, surely Zhang would have been cited for that purpose. Zhang does not disclose or suggest the features that it has been shown above that are not shown by Chong and Ishida, or their combination. Therefore, claim 23 is also patentably distinguishable from Chong, Ishida and Zhang taken alone or in any combination.

**Claims 4 and 5 were rejected by the Examiner under 35 USC §103(a) as being obvious from Chong in view of Talwar.**

Since claims 4 and 5 are each dependent from independent claim 1, they are also patentably distinguishable from Chong as discussed above. Thus for this rejection to stand, Talwar must show or suggest those features that have been shown above to be missing from Chong.

The only reason that the Examiner gives for citing Talwar is to show that the laser specifications of claims 4 and 5 had been used previously. Had the Examiner found any of the features that have been shown to have been missing from Chong, as discussed above, surely Talwar would have been cited for that purpose. Talwar does not disclose or suggest the features that it has been shown above that are not shown by Chong. Therefore, claims 4 and 5 are also patentably distinguishable from Chong and Talwar, or their combination.

While it is possible to distinguish each of the claims from the various combinations of references used in each of the specific rejections cited by the Examiner, given that it has been shown that all of the claims are distinguishable from the primary reference cited in each of the specific rejections it is not necessary to provide the level of detail to show that all of the claims are patentable to the Applicants over all of the



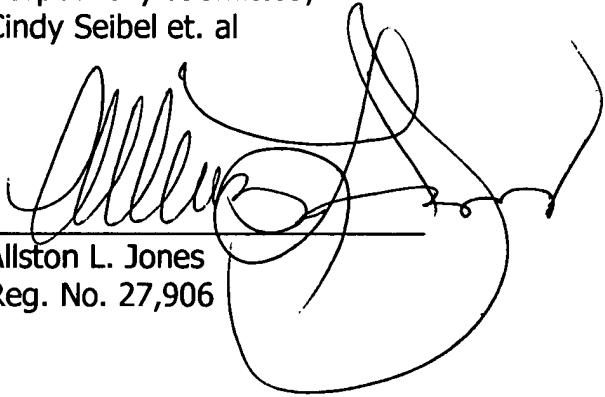
cited references. If it becomes necessary Applicants can distinguish the dependent claims from all of the cited references for many additional reasons.

All claims now being in condition for allowance, their allowance is respectfully requested.

Favorable action is respectfully requested.

Respectfully submitted,  
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